WHAT IS CLAIMED IS:

1. A bus interface unit for transferring data between a plurality of bus devices, said bus interface unit comprising:

1) a first bus device interface comprising: a) a first incoming request bus for receiving request packets from a first one of said plurality of bus devices; b) a first outgoing request bus for transmitting request packets to said first bus device; c) a first incoming data bus for receiving data packets from said first bus device; and d) a first outgoing data bus for transmitting data packets to said first bus device;

2) a second bus device interface comprising: a) a second incoming request bus for receiving request packets from a second one of said plurality of bus devices; b) a second outgoing request bus for transmitting request packets to said second bus device; c) a second incoming data bus for receiving data packets from said second bus device; and d) a second outgoing data bus for transmitting data packets to said second bus device; and

3) an arbitration circuit capable of determining a first priority level associated with a first request packet received from said first bus device and capable of determining a second priority level associated with a second request packet received from said second bus device.

2. The bus interface unit as set forth in Claim 1 wherein said arbitration circuit compares said first priority level and said second priority level to determine which of said first and second priority levels is higher.

3. The bus interface unit as set forth in Claim 2 wherein said arbitration circuit, in response to a determination that said first priority level is higher that said second priority level, causes said bus interface unit to process said first request packet prior to processing said second request packet.

4. The bus interface unit as set forth in Claim 2 wherein said arbitration circuit, in response to a determination that said first priority level is equal to said second priority level, causes said bus interface unit to process said first and second request packets on a rotating turn basis.

5. The bus interface unit as set forth in Claim 1 further comprising a time slice timer capable of producing a current time slice value.

6. The bus interface unit as set forth in Claim 5 wherein said arbitration circuit is capable of determining a fixed time slice range associated with said first bus device and comparing said fixed time slice range with said current time slice value.

7. The bus interface unit as set forth in Claim 6 wherein said arbitration circuit, in response to a determination that said current time slice value is within said fixed time slice range, causes said bus interface unit to process said first request packet prior to processing said second request packet.

8. The bus interface unit as set forth in Claim 7 wherein said arbitration circuit, in response to a determination that said current time slice value is within said fixed time slice range, causes said bus interface unit to process said first request packet prior to processing any pending request packet received by said bus interface unit.

9. An integrated circuit data comprising:

1) N bus devices capable of transferring data with one another; and

2) a bus interface unit for transferring data between said N bus devices, said bus interface unit comprising:

a) N bus interfaces, each of said N bus interfaces comprising: i) an incoming request bus for receiving request packets from one of said N bus devices; ii) an outgoing request bus for transmitting request packets to said one of said N bus devices; iii) an incoming data bus for receiving data packets from said one of said N bus devices; and iv) an outgoing data bus for transmitting data packets to said one of said N bus devices; and

b) an arbitration circuit capable of determining a first priority level associated with a first request packet received from a first bus device and capable of determining a second priority level associated with a second request packet received from a second bus device.

10. The integrated circuit as set forth in Claim 9 wherein said arbitration circuit compares said first priority level and said second priority level to determine which of said first and second priority levels is higher.

11. The integrated circuit as set forth in Claim 10 wherein said arbitration circu

it, in response to a determination that said first priority level is higher that said second priority level, causes said bus interface unit to process said first request packet prior to processing said second request packet.

12. The integrated circuit as set forth in Claim 10 wherein said arbitration circuit, in response to a determination that said first priority level is equal to said second priority level, causes said bus interface unit to process said first and second request packets on a rotating turn basis.

13. The integrated circuit as set forth in Claim 9 further comprising a time slice timer capable of producing a current time slice value.

14. The integrated circuit as set forth in Claim 13 wherein said arbitration circuit is capable of determining a fixed time slice range associated with said first bus device and comparing said fixed time slice range with said current time slice value.

15. The integrated circuit as set forth in Claim 14 wherein said arbitration circuit, in response to a determination that said current time slice value is within said fixed time slice range, causes said bus interface unit to process said first request packet prior to processing said second request packet.

16. The integrated circuit as set forth in Claim 15 wherein said arbitration circuit, in response to a determination that said current time slice value is within said fixed time slice range, causes said bus interface unit to process said first request packet prior to processing any pending request packet received by said bus interface unit.

17. For use in a bus interface unit comprising N bus interfaces, each of the N bus interfaces comprising: i) an incoming request bus for receiving request packets from a corresponding one of N bus devices; ii) an outgoing request bus for transmitting request packets to the corresponding bus device; iii) an incoming data bus for receiving data packets from the corresponding bus device; and iv) an outgoing data bus for transmitting data packets to the corresponding bus device, a method of arbitrating requests received from the N bus interfaces, the method comprising the steps of:

determining a first priority level associated with a first request packet received from a first bus device;

determining a second priority level associated with a second request packet received from a second bus device; and

comparing the first priority level and the second priority level to determine which of the first and second priority levels is higher.

18. The method as set forth in Claim 17 further comprising the step, in response to a determination that the first priority level is higher that the second priority level, of processing the first request packet prior to processing the second request packet.

19. The method as set forth in Claim 17 further comprising the step, in response to a determination that the first priority level is equal to the second priority level, of processing the first and second request packets on a rotating turn basis.

20. The method as set forth in Claim 17 further comprising the step of generating a current time slice value.

21. The method as set forth in Claim 20 further comprising the steps of:

determining a fixed time slice range associated with the first bus device; and

comparing the fixed time slice range with the current time slice value.

22. The method as set forth in Claim 21 further comprising the step, in response to a determination that the current time slice value is within the fixed time slice range, of processing the first request packet prior to processing the second request packet.

23. The method as set forth in Claim 22 further comprising the step, in response to a determination that the current time slice value is within the fixed time slice range, of processing the first request packet prior to processing any pending request packet received by the bus interface unit.